**Faculty of Engineering and Architecture**

**Department of Electrical and Computer Engineering**



**EECE 310L**

**Lab 10 \_ MOS transistor**

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**Section 5**

**Group 1**

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**Table of contents: page**

List of figures……………………………………………………….…..3

Objectives………………………………………………………………4

Lab Equipment used……………………………………………………5

Lab tools used……………………………………………………….….5

Components used…………………………………………………….…5

Experimental Procedure and Discussion……………………………….

1. MOSFET characteristics………………………………………6
2. MOSFET as a voltage controlled resistor……………………..8
3. MOSFET as a logic gate……………………………………..13
4. MOSFET as an amplifier…………………………………….15
5. MOSFET as a current source………………………………...18

References…………………………………………………………......22

Mistakes and Problems faced in the lab…………………………….....23

Signed statement……………………………………………………....24

**List of figures and tables:**

***Tables:***

* Table showing percentage of error in the resistors used (page 5)
* Exercise A part 1 results (page 7)
* Exercise B part 1 results (page 9)
* Exercise B part 2 results (page 9)
* Exercise B part 3 results (page 9)
* Values of RDS corresponding to VGS-VT (page 11)
* Exercise C part 1 results (page 13-14)
* Exercise C part 2 results (page 14)
* Exercise D part 1 results (page 16)
* Exercise D part 2 results (page 16)
* Exercise E results (page 18-19)

***Figures:***

* MOSFET characteristics circuit (page 6)
* MOSFET as a voltage controlled resistor circuit (page 8)
* Plot 1: VGS =VT+2 V (page 10)
* Plot 2: VGS =VT+3 V (page 10)
* Plot 3: VGS =VT+4 V (page 11)
* Field effect transistor (page 12)
* MOSFET as a logic gate circuit (page 13)
* Plot of VOUT vs. VIN1 (page 14)
* Circuit without the amplifier (page 15 left)
* Equivalent circuit representation of the MOSFET circuit as amplifier (page 15 right)
* MOSFET as an amplifier circuit (page 15)
* Measuring delta T for phase shift (page 16)
* MOSFET as current source circuit (page 18 left)
* Equivalent circuit representation of the MOSFET circuit as current source (page 18 right)
* Plot: ID vs. RD (page 19)
* Plot: ID vs. VDS (page 20)
* Ideal ID vs. VDS characteristic for NMOS (page 20)
* Channel regulation (page 21)

**Objectives:**

The objectives of this experiment are to determine the characteristics of the MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) and its applications as a Voltage-controlled resistor, a Logic gate, an Amplifier and a Current source.

**Lab equipments used:**

The equipments that we used are mainly:

* A breadboard
* A power supply
* A digital multimeter (DMM)
* An oscilloscope
* A function generator

**Lab tools used:**

From the toolbox that we have, we only needed:

* the wire stripper
* the wire cutter

**Lab components used:**

We used:

* the BS170 MOSFET
* several resistors of different values
* several capacitors
* connection wires

|  |  |  |
| --- | --- | --- |
| Theoretical value | Measured value | % error |
| 100 Ω | 101.7 Ω | 1.7 % |
| 470 Ω | 472.5 Ω | 0.53 % |
| 1 kΩ | 1.0066 kΩ | 0.66 % |
| 3.3 kΩ | 3.248 kΩ | 1.58 % |
| 4.7 kΩ | 4.68 kΩ | 0.43 % |
| 10 kΩ | 9.843 kΩ | 1.57 % |
| 15 kΩ | 15.125 kΩ | 0.83 % |

**Experimental procedure and discussions:**

1. ***MOSFET characteristics***

*A1.Circuit diagram:*

**

*A2. Detailed experimental procedure:*

**Measurements settings:**

In exercise A, we are trying to find the MOSFET parameters VT (threshold voltage) and k (transconductance). In order to do that, we connected the circuit as shown in the figure above. Not to mention that we used a 100 Ω resistor and the MOSFET. We connected the MOSFET as indicated in its corresponding datasheet. We also supplied a voltage VGG from the power supply = 0.5V. We had to keep the DMM connected as an ammeter to keep track of the value of the current ID. We first kept increasing the VGG so that the current ID would reach the value of 10mA. We recorded the corresponding value of VGS. We did this again until ID reached 25mA.

Knowing that the MOSFET is in saturation region (because VDS=VGS) and having the appropriate formula for ID in this region we could then solve 2 equations with 2 unknowns to calculate k and VT.

Another part from this exercise was to compare the theoretical value of VGS with the experimental value. The experiment here consisted of having the same circuit used before. We just increased VGG to get ID=40mA and recorded the measured value of VGS.

Note here in all part A, we used the DMM to measure both currents and voltages needed (i.e. ID and VGS).

The MOSFET used is an NMOS and this can be seen clearly from its corresponding data sheet.

**Assumptions:**

In this exercise, we had to assume that the MOSFET was in saturation region and use the appropriate equations for it but this was a hypothesis that we proved correct earlier.

The resistor used has 1.7% of error. Not to forget that wires have internal resistances. This fact is not taken into consideration during the theoretical computations.

*A3. Measurements and results:*

*Parts 1 and 2:*

The values obtained for VGS when ID =10 mA and 25 mA are displayed as shown:

|  |  |
| --- | --- |
| ID (mA) | VGS (Volts) |
| 10 | 2.66 |
| 25 | 2.98 |

The equation of ID for the saturation region is: ID = (k/2)(VGS – VT)2

With ID= 10 mA the equation becomes: 10\*10^-3 = (k/2)(2.66-VT)2 (1)

With ID= 25 mA the equation becomes: 25\*10^-3 = (k/2)(2.98-VT)2 (2)

(2)/(1) => 2.5= (2.98-VT)2 / (2.66-VT)2

 => √2.5 = (2.98-VT)/ (2.66-VT)

 => √2.5\*(2.66-VT) = 2.98- VT

 => VT= 2.086 V

Replacing the value of VT in equation (1) => 10\*10^-3 = (k/2)(2.66-2.086)2

=> k= (2\*10\*10^-3)/ (2.66-2.086)2

=> k=0.06287 A/ V^2 = 62.87 mA/ V^2

*Part 3:*

**Theoretical calculations:**

We know that VGS = VT + √ (2ID / k)

We want the value of VGS when ID= 40 mA and we already know the values of VT and k (calculated in part 1 and 2).

Therefore VGS = 2.086 + √((2\*40\*10^-3)/0.06287) = 3.214 V

**Experimental results:**

After increasing VGG in order to get ID= 40 mA we were able to read on the DMM that VGS=3.25 V.

**Comparison and %error:**

The theoretical value for part 3 is: 3.214 V

The experimental value obtained is: 3.25 V

The 2 values were so close which means that the measurements were correct and relatively precise but that doesn’t exclude the fact that we have experimental errors such as errors in the equipments or human errors.

The percentage of error is: [(3.25-3.214)/3.214] \*100 = 1.12%

1. ***MOSFET as a voltage-controlled resistor***

*B1. Circuit diagram:*



*B2. Detailed experimental procedure:*

**Measurements settings:**

For this exercise, we connected the same MOSFET with a 1kΩ resistor and provided 2 dc voltages from the power supply VDD and VGG. We connected the circuit as shown in the figure above. Note that we kept the ammeter (DMM) connected during all the experiment to measure ID. the oscilloscope is used to measure VGS and VDS.

In part 1, we set VGG=VT+2 = 2.086+2= 4.086V. This value is equal to VGS because we have IG=0. Then we regulated VDD so we get VDS = 0.1V. We kept measuring ID for several values of VDS.

In parts 2 and 3, we set VGG=VT+3V and VGG=VT+4V and repeated the same measurements as part 1.

**Assumptions:**

In this exercise, we had to assume that the MOSFET was in triode region (also called linear or ohmique). This can be proven because we had VGS>VT and VDS< VGS-VT during this exercise.

*B3. Measurements and results:*

**Theoretical calculations:**

In this exercise we did not do any calculations based on formulas given we just recorded experimental values and results.

**Experimental results:**

*Part1:*

The values obtained when VGS =VT+2 = 2.086+2= 4.086V are as shown:

|  |  |
| --- | --- |
| VDS (Volts) | ID (mA) |
| 0.1 | 6.95 |
| 0.15 | 10.8 |
| 0.2 | 13.74 |
| 0.25 | 17.45 |
| 0.3 | 20.85 |

*Part 2:*

The values obtained when VGS =VT+3 = 2.086+3= 5.086V are as shown:

|  |  |
| --- | --- |
| VDS (Volts) | ID (mA) |
| 0.1 | 77.5 |
| 0.15 | 94.53 |
| 0.2 | 136 |
| 0.25 | 164 |
| 0.3 | 197 |

*Part 3:*

The values obtained when VGS =VT+4 = 2.086+4= 6.086V are as shown:

|  |  |
| --- | --- |
| VDS (Volts) | ID (mA) |
| 0.1 | 81 |
| 0.15 | 103 |
| 0.2 | 156 |
| 0.25 | 174 |
| 0.3 | 226 |

*B4. Discussion:*

* Plot 1: VGS =VT+2 V

 ****

Plot 2: VGS=VT+3 V



Plot 3: VGS= VT+4 V

 

* These graphs look almost as a straight line. But this is not the case due to some errors in the values that prevent the graphs from being perfectly linear.
* Slope for plot 1: (20.85-6.95)/(0.3-0.1) = 69.5 mA/V = 0.0695 A/V

Slope for plot 2: (197-77.5)/(0.3-0.1)= 597.5 mA/V= 0.5975 A/V

Slope for plot 3: (226-81)/(0.3-0.1)= 725 mA/V= 0.725 A/V

* We know that R=1/slope

R1 (corresponding to plot 1) =1/0.0695= 14.39Ω

R2 (corresponding to plot 2) =1/0.5975= 1.67Ω

R3 (corresponding to plot 3) =1/0.725= 1.38Ω

|  |  |
| --- | --- |
| VGS-VT (V) | RDS (Ω) |
| 2 | 14.39 |
| 3 | 1.67 |
| 4 | 1.38 |

The value of R depends on VGS-VT.

* The MOSFET is biased in the triode region which is also called linear or ohmiquebecause VGS>VT and VDS< VGS-VT in all the 3 parts of this exercise.
* This region is called linear because in this region we have that RDS=VDS/ ID which is a linear relation between the VDS and ID. And it is called ohmique because the MOSFET acts as a voltage controlled resistor in this region.
* ID = (k/2)(2(VGS – VT) VDS – VDS2 )
* This equation has the form of ID= constant \* VDS (we can ignore VDS2 because it is small: order of 10^-2 ) which is a linear relation between ID and VDS. this is the case of the voltage controlled resistor behavior knowing that the constant is equal to GDS=1/RDS.
* Error= (ID approximation - ID)/ID <5/100

ID approximation is the expression where we neglect the squared term because it’s very small. ID approximation =(k)(VGS-VT)VDS

=>( k(VGS-VT)VDS - k(VGS-VT)VDS + (k/2) VDS2)/((k/2)(VGS-VT)VDS-VDS2)<5/100

=> ((k/2) VDS2 )/ (k(VGS-VT)VDS – (k/2)VDS2) < (5/100)

=> (VDS2/2)/(VDS(VGS-VT) – (VDS2/2)< 5/100 simpifiying by VDS and arranging

=> (21/40)VDS < (5/100)(VGS-VT)

=> VDS<0.952(VGS-VT)

* Replacing the values of part 1 in the equation of ID, we get:

ID= (0.06287/2)(2(2)VDS - VDS2)

We can by approximation eliminate VDS2 because it is very small.

=> ID=0.12574 VDS

=> RDS= VDS/ID = 8Ω

R(theoretical)=8Ω < R(experimental)=14Ω

Error= (14-8)/8 = 0.75 = 75%

* We encounter voltage controlled resistors mostly as FET (field effect transistor). It has applications is several domains such as:
* Attenuators
* Amplifiers
* Modulation circuits
* Filters
* Oscillators
* Audio and video applications
* Automatic gain controls
1. ***MOSFET as logic gate***

*C1. Circuit diagram:*



*C2. Detailed experimental procedure:*

**Measurements settings:**

In this exercise we connected 2 MOSFETS (of the same type) with a 470 Ω resistor. In addition to this we supplied a fixed voltage VDD=5V. The circuit was connected as shown above. We recorded the values of voltages VIN1, VIN2 and VOUT. This was done using a DMM.

Note that in this exercise, the circuit behaves as a logic gate. We will observe its truth table later.

**Assumptions:**

In order to operate as a switch or a logic gate, the MOSFET should be operating between the triode (or linear) region and the cut-off.

The resistor used in this exercise has 0.53% of error. Plus, Wires have internal resistances. This fact is not taken into consideration during the theoretical computations.

*C3. Measurements and results:*

*Part1:*

We supplied some combinations of logic 1 and logic 2 across input 1 and 2. We get the following truth table and corresponding voltages:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| IN1 (logic) | IN2 (logic) | OUT (logic) | VIN1 (V) | VIN2 (V) | VOUT (V) |
| 0 | 0 | 1 | 0 | 0 | 4.99 |
| 0 | 1 | 0 | 0 | 4.99 | 0.14 |
| 1 | 0 | 0 | 4.99 | 0 | 0.02 |
| 1 | 1 | 0 | 4.99 | 4.99 | 0.015 |

To have logic 0, we connect the terminal wanted to ground. To have logic 1, we connect the wanted terminal to VDD.

After looking at this truth table we can say that this circuit implements a NOR gate.

*Part2:*

After setting VIN2=0 we vary the values of VIN1 and record the values of VOUT. The results are displayed in the following table:

|  |  |  |  |
| --- | --- | --- | --- |
| VIN1 (V) | VOUT (V) | MOSFET region | Logic value |
| 0 | 4.98 | Cut-off | 1 |
| 1.2 | 4.98 | Cut-off | 1 |
| 2.4 | 0.04153 | triode | 0 |
| 3.6 | 0.02191 | saturation | 0 |

*C4. Discussion:*

* The value of the voltage corresponding to logic 1 for this MOSFET is approximately =5V. While the value of the voltage corresponding to logic 0 is approximately=0V.
* We notice that the values obtained for logic 0 are slightly higher than 0. This is due to the resistor that is connected. Also, when increasing the resistance the low voltage output will decrease.
* Plot of VOUT vs. VIN1:



* The output switches at VIN1= 2.4V
1. ***MOSFET as an amplifier***

*D1. Circuit diagram:*





*D2. Detailed experimental procedure:*

**Measurements settings:**

In this exercise, we connected 6 resistors, 3 capacitors, the MOSFET, and the function generator supplying 100 mV peak-to-peak, 10 kHz sine signal as shown in the above circuit. We observed the input and output voltages VS and VO respectively on the oscilloscope.

Note that capacitors C1 and C2 were used as coupling capacitors to eliminate the DC offset. Whereas CS was used as a bypass capacitor that acts as a short circuit at high frequencies and thus shorts RS2.

**Assumptions:**

In this exercise, we had to assume that the MOSFET was in saturation region in order to operate as an amplifier.

Resistors have each a percentage of error and wires have internal resistances. This fact is not taken into consideration during the theoretical computations.

*D3. Measurements and results:*

*Part 1:*

After connecting the circuit inside the dotted box, we recorded the DC values of ID, VGS and VDS. The results came as following:

|  |  |  |
| --- | --- | --- |
| ID (mA) | VGS (V) | VDS (V) |
| 2.35 | 4.73 | 9.59 |

*Part 2:*

In this part we connected the whole circuit and recorded the peak to peak values of VS (input voltage from voltage source), VI (input voltage of the amplifier) and VO (output voltage) as shown:

|  |  |  |
| --- | --- | --- |
| VS pk-pk (mV) | VI pk-pk (mV) | VO pk-pk (mV) |
| 113 | 64 | 720 |

We also measured the phase shift between VO and VI using the oscilloscope.

To measure ΔT we adjust the 2 probes of VO and VI on the oscilloscope screen to have them superposed and aligned on the same horizontal axis. This can be done by modifying VOLT/DIV and SEC/DIV settings. Now ΔT can be clearly deduced from the difference between 2 points selected as shown:



T is the period of a signal. In this case, both signals have same T. we measure it on the oscilloscope. Note that we can obtain T if we already know the frequency by simply using the formula: T= 1/F

Experimentally, we found that the phase angle =180O

Whereas theoretically, the phase angle is also = 180O caused by the minus sign found in the formula of the gain of this special amplifier. Gain= VO/VI= -g\*RD

We can see that the error here between the theoretical value and the experimental value is 0 due to the precision of the oscilloscope.

We can conclude from the table above that:

Voltage gain = -VO/VI= -720/64= -11.25 V/V. The gain is negative because we got a phase shift of 180 degrees.

Current gain = IO/II = (VO/VI)(𝑅𝑠||𝑅𝐺1)/ RL = -12.2 A/A

Power gain = voltage gain \* current gain = 137.25 W/W

*Part 3:*

In this part, we found the bandwidth of the amplifier by finding its two cut-off frequencies.

This was done by increasing then decreasing the value of the frequency till VO reaches a value= VO at mid frequencies / √2. We found the following result:

Flow=308 Hz

Fhigh= 250 kHz

*D4. Discussion:*

* At low frequencies the capacitor acts as an open circuit. This means that C2 reduces the output voltage and therefore the gain drops.

At very high frequencies the capacitor acts as a short circuit, but the gain drops also because at high frequencies, the MOSFET will no longer be in the saturation region and therefore will not work properly as an amplifier.

* When the block is connected, if we increase the amplitude of the input, then this will cause the MOSFET to exit the saturation region and enter the linear region. And since we know that the MOSFET works as an amplifier only in saturation region then we should expect that the resulting output will be distorted. Whereas in the case when the block is not connected we will not face this problem and won’t have distortion.
1. ***MOSFET as a current source***

*E1. Circuit diagram:*



*E2. Detailed experimental procedure:*

**Measurements settings:**

In this exercise we used a MOSFET and 4 resistors of different values. We supplied a voltage VDD=10V. The circuit was connected as shown in the figure above (on the left).

In this circuit the MOSFET behaves as a current source. The equivalent circuit is shown in the figure above (on the right).

We put different values of RD and measured the resulting current ID and voltage VDS using a DMM.

**Assumptions:**

In this exercise, we had to assume that the MOSFET was in saturation (IG=0). Resistors have each a percentage of error and wires have internal resistances. This fact is not taken into consideration during the theoretical computations.

*E3. Measurements and results:*

**Experimental results:**

The results are shown in this table:

|  |  |  |
| --- | --- | --- |
| RD (Ω) | ID  (mA) | VDS (mA) |
| 0 | 9.85 | 9.9 |
| 100 | 9.83 | 7.9 |
| 220 | 9.81 | 6.8 |
| 330 | 9.8 | 5.7 |
| 470 | 9.78 | 4.4 |
| 560 | 9.76 | 3.56 |
| 680 | 9.7 | 2.54 |
| 820 | 9.67 | 1.17 |
| 1000 | 9.63 | 0.25 |

 **Choosing the correct value of R2:**

Knowing that the MOSFET is in the saturation region, we have that:

ID = (k/2)(VGS – VT)2 (1)

By KVL we can deduce the following equation:

VR2= VGS+ISRS= (R2/R2+R1)\*VDD (2)

Setting ID= 10 mA in (1), we can retrieve the value of VGS. For VT and k we use the values calculated in exercise A.

=> 10\*10^-3= (0.06287/2)\*(VGS-2.086)2

=> VGS-2.086=0.564

=> VGS= 2.65V

Replacing the value of VGS in (2) we get:

=> 2.65+10\*10-3 \*100= (10R2/R2+10\*10^3)

=> 3.65= (10R2/R2+10\*10^3)

=> R2+10\*10^3=36.5R2

=> R2= 281.69Ω

*E4. Discussion:*

* Plot of ID vs. RD:

 

 The MOSFET behave as a current source where the plot of ID vs. RD slightly decreases, before the region having a high slope. In this case it’s between 0 and 330 Ω.

* IS=10 mA
* Plot of ID vs. VDS:



The region is between VDS=4.4V and VDS=9.9 V. In this region ID changes slightly.

This is the saturation region of the MOSFET.

 This can be easily seen from an ideally shaped curve and after fitting the points of our curve into the a logarithmic approximation :





* In reality the ID vs. VDS curve have an inclined line in the saturation region with a certain slope >0 (which was the ideal case) this is explained in the following figure:



As shown in the figure, ro=1/(slope of the saturation region)

In our plot, slope= ((9.85-9.8)\*10^-3)/ (9.9-5.7) =1.19\*10^-5

=> ro= 1/ (1.19\*10^-5)= 84kΩ

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**Mistakes and problems faced in the lab:**

One of the few mistakes that we encountered during this lab was that we were given a burnt MOSFET. Our results were all wrong. We had to replace it with another one and redo all the work.

Another thing was that the wires of the oscilloscope were not functioning properly and we had to replace them also so we can get a correct output.

*“I HAVE NEITHER GIVEN NOR RECEIVED AID ON THIS REPORT NOR HAVE I CONCEALED ANY VIOLATION OF THE AUB STUDENT CODE OF CONDUCT.”*



 Emilie Y. Akiki